BINDURA UNIVERSITY OF SCIENCE EDUCATION

FACULTY OF SCIENCE EDUCATION

DEPARTMENT OF ENGINEERINGAND PHYSICS

Bachelor of Science Honours Degree in Electronic Engineering

EEE1207 - Digital Electronics

JUN 2025

Time Allowed: 3 Hours **Total Marks:100**

Special Requirements: Scientific Calculator, rule, pen, pencil

INSTRUCTIONS

1. Answer any **FIVE (5) questions**

2. The question paper **contains SEVEN (7)** questions

2. Each question carries 20 marks

1(a) Using waveform diagrams, differentiate a analogue signal from a digital signal [4]

(b) State three advantages of digital signals over digital signals [3]

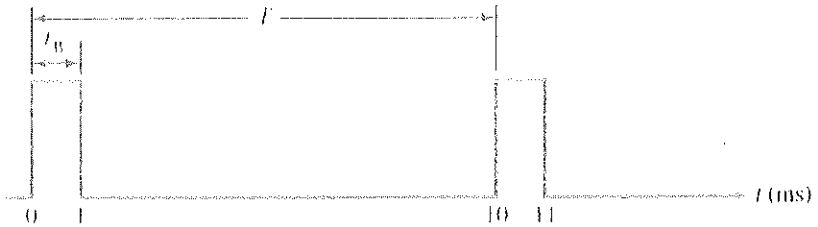
(c) Using a well labelled diagram suitable explain what a non-ideal pulse looks like.

(i) A circuit has a bandwidth of 200 kHz. What is the fastest rise time this circuit will pass? [2]

(ii) A pulse train has a rise time of 6 ns. What is the minimum bandwidth to pass this pulse train faithfully? [2]

(d) Give examples of two analogue and two digital systems

(e) A portion of a periodic digital waveform is shown in Figure below. The measurements are in milliseconds.



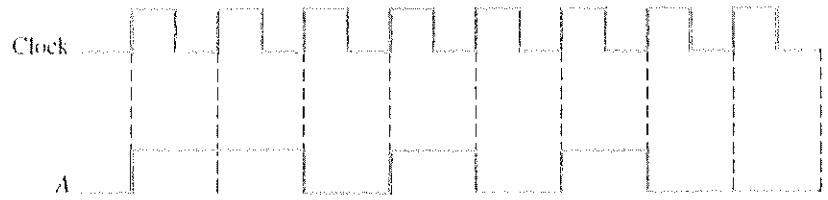
Determine the following:

(i) period [1]

(ii) frequency [1]

(iii) duty cycle [2]

f) (i) Determine the total time required to serially transfer the eight bits contained in waveform *A* of Figure below. The 1 MHz clock is used as reference. [2]



(ii) What is the total time to transfer the same eight bits in parallel? [1]

(ii) A parallel transfer would take 1 mS for all eight bits.

(g)Draw a timing diagram for a digital signal that continuously alternates between 0.2 V (binary 0) for 2 ms and 4.4 V (binary) for 4 ms. [2]

2(a)Find the equivalent of the following numbers

(i) decimal equivalent of $(1E0.2A)_{16}$ [2]

(ii)decimal equivalent of 137.21_8 [2]

(iii)hexadecimal equivalent of 82.25_{10} [2]

(iv)octal equivalent of $2F.C4_{16}$ [2]

(v)and the hex equivalent of 762.013_8 [2]

(b) Find 2's complement of 00011101. [2]

(c)(i)State two advantages of Gray Code and its disadvantage. [2]

(ii)Encode the decimal number 46 to Gray code. [2]

(iii)Convert 1010010 to Gray Code. [2]

(iv)Convert Gray code word 1111011 into binary [2]

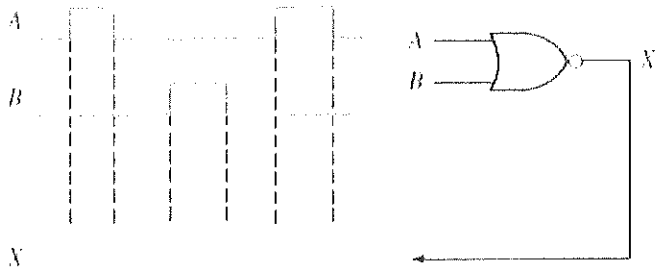
3(a)(i) Represent a NOR gate using ON/OFF switches, bulb and a cell [2]

(ii)Derive the truth table for the NOR gate [2]

(iii)Give the logic symbol of a NOR gate [1]

(iv)Write down a Boolean expression of the above NOR gate [1]

(b)If the two waveforms shown in Figure are applied to a NOR gate, what is the resulting output waveform? [2]



(c)(i) State two De-Morgen's Theorems using Boolean algebra [1]

(ii)Prove the two theorems using truth tables [4]

(d) Apply De-Morgan's theorem to the expression [5]

$$\overline{\overline{AB}(CD + \bar{E}F)(\overline{AB} + \overline{CD})}$$

(e)Derive Boolean expression from the truth table below [2]

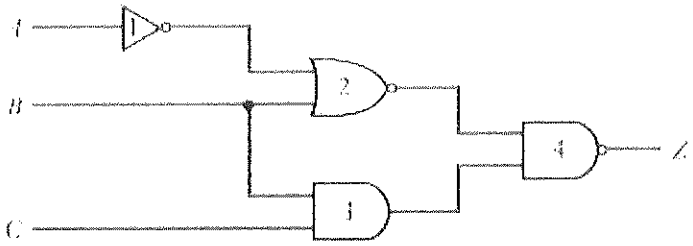
A	B	C	x
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

4(a)Implement use NOR gates only the expression $Y = \bar{A}B + \bar{B}C$ [5]

(b)Design a logic circuit that has three inputs, *A*, *B*, and *C*, and whose output will be HIGH only when a majority of the inputs are HIGH. [5]

(c) In a simple copy machine, a stop signal, *S*, is to be generated to stop the machine operation and energize an indicator light whenever either of the following conditions exists: (1) there is no paper in the paper feeder tray; or (2) the two microswitches in the paper path are activated, indicating a jam in the paper path. The presence of paper in the feeder tray is indicated by a HIGH at logic signal *P*. Each of the microswitches produces a logic signal (*Q* and *R*) that goes HIGH whenever paper is passing over the switch to activate it.
Derive a truth table from the given conditions. **[5]**

(d)Derive a Boolean expression for the logic circuit below. **[2]**



(e)Implement the following Boolean expression $Y = \bar{A}B + \bar{B}C$ using NOR gates only. **[3]**

5(a) Minimize the expression Y = F(A,B,C) = $\bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}BB + A\bar{B}C$ using Karnaugh map. **[5]**

(b)(i)Explain the operation of a 4-to-1 multiplexer with the aid of a logic circuit.**[5]**

(ii)Derive the truth table for the for the multiplexer **[5]**

(c)Draw the logic circuit diagram of a two-bit Ripple Up-counter using Negative Edge-triggered Flip-flops **[2]**

(d)Explain its operation using a timing diagram **[3]**

6(a) What is the difference between level and edge triggering. **[2]**

(b)(i) Draw a logic diagram of a clocked SR flip-flop using NAND gates. **[3]**

(ii)Describe its operation with the aid of its truth table. **[2+2]**

(c)Draw the logic symbol of a positive triggered JK flip-flop **[3]**

(d)How can a S-type flip-flop be converted to a D-type flip-flop **[2]**

(e)With the aid of block diagrams outline the main difference between combinational and sequential logic circuits. **[3+3]**

7(a) Why is a flip flop called a shift register **[2]**

(b)With the aid of block diagrams illustrate the basic movement of data using 4 bits in the four types of shift registers. **[2+2+2+2]**

(c)Assume that a 4-bit counter starts in the 0000 state. What will be the count after 12 input pulses? **[2]**

(d)Draw a logic diagram for 3-stage triggered asynchronous counter with negative triggered flip-flops. **[6]**

(e)A counter has 14 stable states 0000 through 1101. If the input frequency is 50 KHz, what will be its output frequency. **[2]**

THE END