**BINDURA UNIVERSITY OF SCIENCE EDUCATION**

**PHYSICS AND ENGINEERING DEPARTMENT**

**PH115: DIGITAL LOGIC**

JUN 2023

**TIME: 3 HOURS**

**INSTRUCTIONS**

Answer **question one** in Section A and **any three** questions from Section B. Section A carries 40 marks and each question in Section B carries 20 marks.

**SECTION A**

1. a. Concisely describe the major differences between analogue and digital quantities. [4]

b. i. What is the next binary number following $10111_2$ in the counting sequence? [2]

ii. What is the largest decimal value that can be represented using 12 bits? [2]

c. Convert the following binary coded decimal (BCD) number to its decimal Equivalent: 0110100000111001. Comment on you finding. [5]

d. i. What is a truth table? [2]

ii. What is the only set of input condition that will produce a LOW output for any OR gate? [2]

e. i. What is the advantage of a synchronous counter over an asynchronous Counter? What is the disadvantage? [4]

ii. How many logic devices are required for a MOD-64 parallel counter? State them. [4]

iii. What Logic signal drives the J, K. inputs of the MSB flip-flop for the counter in 1(e)(ii)? [2]

f. Define the following terms:

i. Magnitude comparator [3]

ii. Multiplexers [3]

iii. Demultiplexers [3]

g. iv. Distinguish between a *serial in/parallel out* register and a *serial in/serial out* register. [4]

**SECTION B**

2. a. State whether each of the following is a digital or analogue quantity:

i. Number of atoms in a sample of material [1]

ii. Altitude of an aircraft [1]

iii. Pressure in a bicycle tyre [1]

iv. Current through a speaker [1]

v. Time setting on a microwave [1]

b. Draw a timing diagram for a digital signal that continuously alternates between 2.0V (binary 0) for 2milli-seconds (ms) and 4.4V for 4ms. [5]

c. Convert each of the following octal numbers to its decimal equivalent:

i. 36 [1]

ii. 1655 [1]

ii. 1204 [1]

iv. 5 [1]

d. Convert each of the following decimal numbers to octal: [1]

i. 372 [1]

ii. 771 [1]

ii. 255 [1]

e. Convert each of the following octal values to binary:

i. 36 [1]

ii. 1655 [1]

ii. 1204 [1]

3. a. Write the expression for the output of figure 1, and use it to determine the complete truth table. [6]

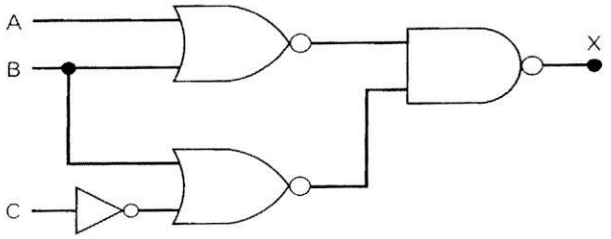


Figure 1: Combinational circuit

b. i. Show how a two-input NAND gate can be constructed from two-input NOR gates. [4]

ii. Show how a two-input NOR gate can be constructed from two-input NAND gates. [4]

c. Under what conditions will:

i. an OR gate allows a logic signal to pass through to its output unchanged? [2]

ii. an AND gate allows a logic signal to pass through to its output unchanged? [2]

iii. a NOR gate allows a logic signal to pass through to its output unchanged? [2]

4. a. i. Draw a NAND Latch and its truth table. For a NAND Latch what is the Normal state of the $\overline{SET}$ and $\overline{CLEAR}$ inputs? [8]

b. Add the following in binary. Check your results by doing the addition in decimal.

i. 1010 + 1011 [2]

ii. 1111 + 0011 [2]

iii. 1011.1101 + 11.1 [2]

iv. 0.1011 + 0.1111 [2]

c. Find the sum of each of the following pairs of hex numbers:

i. 3E91 + 2F93 [2]

ii. 91B + 6F2 [2]

5. a. In figure 2 below change each AND gate to an OR gate, and change the OR gate to an AND gate. Then write its expression for output x [4]

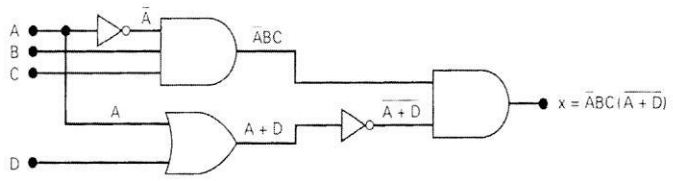


Figure 2: Combinational Logic expression

b. Draw the circuit diagram to implement the expression: x=(A+B) ($\bar{B}$+C). Explain how you figure out. [4]

c. i. State the two general forms for logic expressions. [2]

ii. Outline the approach or steps you would take to design a combinational logic circuit. [4]

d. Clearly distinguish between an exclusive-OR and an exclusive-NOR circuit by their respective expressions and stating when each of them has HIGH output. [6]

6. a. What is meant by the following:

i. D Latch circuit [3]

ii. A one-shit. [3]

b. Outline principal uses of FFs [5]

c. What are the effects of a Schmitt-trigger type of input to a circuit? [5]

d. Give the meaning of the following digital system terms:

i. Data bus [2]

ii. Tristate outputs [2]

**END OF EXAMINATION**