BINDURA UNIVERSITY OF SCIENCE EDUCATION

FACULTY OF SCIENCES

DEPARTMENT OF ENGINEERING AND PHYSICS

DIGITAL DEVICES AND SYSTEMS

EEE 2205

Examination Paper [1]

This examination paper consists of 3 pages

Time Allowed: 3 hours

Total Marks: 100

Special Requirements: Calculator

INSTRUCTIONS

1. Answer any FOUR questions only.
2. Each question carries 25 marks.
3. Show your steps clearly in any calculation.
4. Start the answers for each question on a fresh page.

MARK ALLOCATION

QUESTION	MARKS
1.	25
2.	25
3.	25
4.	25
5.	25
6.	25
TOTAL	100

Question 1

(a) Describe and differentiate two types of counters depending on clock pulse applied. [10 Marks]

(b) Design a 4- bit Asynchronous Up Counter, showing the count truth table to the eighth state as well the timing diagrams using falling edge triggered. [15 Marks]

Question 2

Flip flops are used as one bit storage devices. Using a NAND gates explain how the JK Master slave using truth tables and diagrams. [25 Marks]

Question 3

(a) In many digital circuits, flip flops can be used for frequency division. How many flip flops are required to count from 0 to 512. [5 marks]

(b If a 4 bit counter is supplied a clock frequency of 1MHz, what will be the frequency of the last counter. Using negative edge triggering to illustrate timing diagrams show your answer. . [10 marks]

c) What is the role of registers in digital systems? Explain one method of how these can be used to store 8 bits of data. [10 marks]

Question 4

(a) What is a trigger pulse? Using diagrams explain the two accurate methods of triggering [10 Marks]

b) The advantages of the Synchronous counter over asynchronous counter [10 Marks]

c) What is a Counter? [5 marks]

Question 5

(a) Briefly discuss, what is dynamic memory? [5 marks]

(b)

i. Two types of memory are commonly implemented in computer systems. These are the RAM and the ROM. Define each memory and distinguish the differences between the two. [5 marks]

ii. Suggest any applications where each memory would be ideal justifying your answer. [5 marks]

c) Using combinational logic circuits, design a 4 bit subtractor clearly explaining how it works with the use of a truth table. [10 Marks]

Question 6

Design a 4 bit PIPO shift register falling edge triggered. Show the timing diagrams and truth tables. [25 Marks]