BINDURA UNIVERSITY OF SCIENCE EDUCATION
FACULTY OF SCIENCE AND ENGINEERING
DEPARTMENT COMPUTER SCIENCE
BSc HONS DEGREE IN COMPUTER SCIENCE DEGREE/INFORMATION TECHNOLOGY

COURSE CODE CS113/NWE114/SWE203: COMPUTER ARCHITECTURE

DURATION: 2 HOURS 30 MINUTES TOTAL MARKS: 100

INSTRUCTIONS TO CANDIDATES

OCT 2024

This paper contains five questions
Answer all questions.

Question 1

a) A digital computer has a memory unit with 32 bits per word. The instruction set consists of 110 different operations. All instructions have an opcode and two address fields: one for a memory address and one for a register address. This particular system includes eight general purpose, user addressable registers. Registers may be loaded directly from the memory, and memory may be uploaded directly from the registers. Direct memory-to-memory data movement operations are not supported. Each instruction is stored in one word of memory.

i) How many bits are needed for the opcode? [2]
ii) How many bits are needed to specify the register? [2]
iii) How many bits are left for the memory address part of the instruction? [2]
iv) What is the maximum addressable size for memory? [4]

b) Show how the following floating point value -142.625 would be stored using IEEE-754 single precision. [10]

Question 2

a) Some people use a computer's clock speed to judge the performance (speed) of a computer; for example, they may say that computer X is better than computer Y because computer X has a 4.0 GHz clock and computer Y has a 2.0 GHz clock. In general, it is regarded as wrong to use clock frequency to compare computers. Why is this? **[6]**

b) Consider the following two processors P1 and P2 executing the same instruction set with the clock rates and CPIs specified in table 1.

Processors	Clock rate	CPI
P1	2GHz	1.0
P2	3GHz	2.5

Table 1: Processor performance data

i) Suppose we would like to compare the performance of the two processors, suggest any metric that we can use considering the data in the table. **[2]**

ii) Which processor has the higher performance? (show working) **[6]**

iii) If the processors each execute a program in 100 seconds, find the number of cycles and the number of instructions for each processor. **[6]**

Question 3

a) With the aid of a diagram, describe what is meant by *instruction pipelining*, and explain how it can be used to improve CPU performance. **[6]**

b) By using sample programs, explain the causes of the following types of pipeline hazard and outline briefly how their effects on performance can be minimized.

i. Data hazards **[6]**

ii. Control hazards **[6]**

c) How can the effects of structural hazards be minimized, taking into consideration the price of a general purpose machine? **[2]**

Question 4

i. Explain the principles that cache memory relies on to optimize its performance? **[6]**

ii. Explain the similarities and differences between polled I/O and interrupt driven I/O. **[6]**

iii. Would a microprocessor be able to function without interrupts? Explain. **[2]**

iv. What would be the effect, if any? Explain. **[2]**

v. In some ways an interrupt is similar to a subroutine call. In what ways are interrupts are subroutine calls similar and in what ways do they differ? **[4]**

Question 5

a) Why should assembly language be avoided for general application development? Under what circumstances is assembly language preferred or required? **[4][2]**

b) Translate the following c/c++ statements, which are just part of a much larger program, into an equivalent sequence of MIPS assembly instructions. You should assume that this is a complete MIPS assembly program and the integer variables x and y are in registers. Initially, upon program loading, the value of x is 0 and the value of y is 0. **[14]**

```
y= 10
while (x<y) {
    if (x==0)
        x = x + 1
      else
        x = x * 2

      }
```

END OF PAPER