BINDURA UNIVERSITY OF SCIENCE EDUCATION
FACULTY OF SCIENCE AND ENGINEERING
DEPARTMENT COMPUTER SCIENCE
BSc HONS DEGREE IN COMPUTER SCIENCE DEGREE/INFORMATION TECHNOLOGY

COURSE CODE CS113/NWE114/SWE203: COMPUTER ARCHITECTURE

DURATION: 2 HOURS 30 MINUTES TOTAL MARKS: 100

INSTRUCTIONS TO CANDIDATES

This paper contains five questions
Answer all questions.

---

## Question 1

a) Write the following number -213.725 as a 32-bit, IEEE normalized floating point number with biased exponent. Show all your work. **(10 marks)**

b) Why the exponent is stored as a biased exponent instead of the usual two's complement notation? **(2 marks)**

## Question 2

a) How is instruction pipeline widely used to enhance performance of modern computers? **(8 marks)**

b) Consider the following code fragment in figure 1.1:

```
                li      $s1,1
                li      $s3,6
                add     $s4,$zero,$zero
outer_loop:     beq     $s1,$s3,done
                add     $s2,$zero,$zero
inner_loop:     addi    $s2,$s2,1
                mul     $t0,$s2,$s1
                add     $s4,$s4,$t0
looptest:       bne     $s2,$s1,inner_loop
                addi    $s1,$s1,1
                j outer_loop
done:
```

Figure 1.1: Code Fragment

Calculate (using the Gantt's chart) the number of cycles needed to execute the above code if the pipeline described above is used. **Assume that there is no forwarding hardware** and that when branch instructions are fetched; the pipeline will "stall" until the target address is calculated and the branch decision is made.

**(15 marks)**

## Question 3

a) What are the von Neumann architecture principles and how do they lead to the von Neumann bottleneck? **(6 marks)**

b) How does the cache memory attempt to reduce the effects of the von Neumann bottleneck? **(6 marks)**

c) Explain the cache memory's write through and write back policies. **(6 marks)**

d) Which strategy offers a better performance and why? **(2 marks)**

e) A computer makes 95% of its memory accesses to cache memory with an access time of 10 ns, it makes 4.9% of its accesses to main memory with a 50 ns access time, and it makes 0.1% of its accesses to a disk drive with a 4 ms access time. What is the average memory access time? **(6 marks)**

## Question 4

a) A particular instruction set has five categories of instruction as shown in figure 1.2. For a hardware implementation, instructions in each category take the number of cycles shown below. Also a certain machine code program contains the following proportions of instructions from the five categories:

| Type | A | B | C | D | E |
|---|---|---|---|---|---|
| CPI | 1 | 3 | 2 | 5 | 1 |

| Type | A | B | C | D | E |
|---|---|---|---|---|---|
| Proportion | 20% | 30% | 25% | 20% | 5 |

**Figure 1.2: Categories of instructions**

i) Calculate the average CPI for this program. **(6 marks)**

ii) Given that the CPU has a clock rate of 200MHz, determine the execution time for this program? **(6 marks)**

b) Suppose a program consists of 40% floating point multiply instructions, 20% floating point divide instructions, and the remaining 40% are other instructions. Floating point division, floating point multiplication, and each of the other instructions have the same CPI. What speedup would be achieved, for this program, if floating point multiplication were made 2 times faster and floating-point division made 4 times faster? **(6 marks)**

## Question 5

a) Given the wide use of High Level Languages (HLL) today, is there still need for assembly languages in the software development industry? **(6 marks)**

b) Write a complete MIPS assembly program implementing following high-level language pseudo-code, where the variables a and b are numbers entered from the keyboard and print the final result of b on the screen as shown in figure 1.3. **(15 marks)**

```
int a = X
int b = Y
if (a and b are positive)
    {
      while a > 0
       do
       {
        b := a^2 + b^2;
        a := a - 1;
        }
    }
```

**Figure 1.3: High level language pseudo code**

**END OF PAPER**